SONY

CXP82032/82040/82052/82060

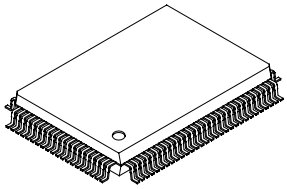
CMOS 8-bit Single Chip Microcomputer

Description

The CXP82032/82040/82052/82060 is a CMOS 8-bit single chip microcomputer integrating on a single chip an A/D converter, serial interface, timer/counter, time-base timer, capture timer/counter, fluorescent display panel controller/driver, remote control reception circuit, and PWM output besides the basic configurations of 8-bit CPU, ROM, RAM, and I/O port.

The CXP82032/82040/82052/82060 also provides sleep/stop function that enables lower power consumption.

100 pin QFP (Plastic)



Structure

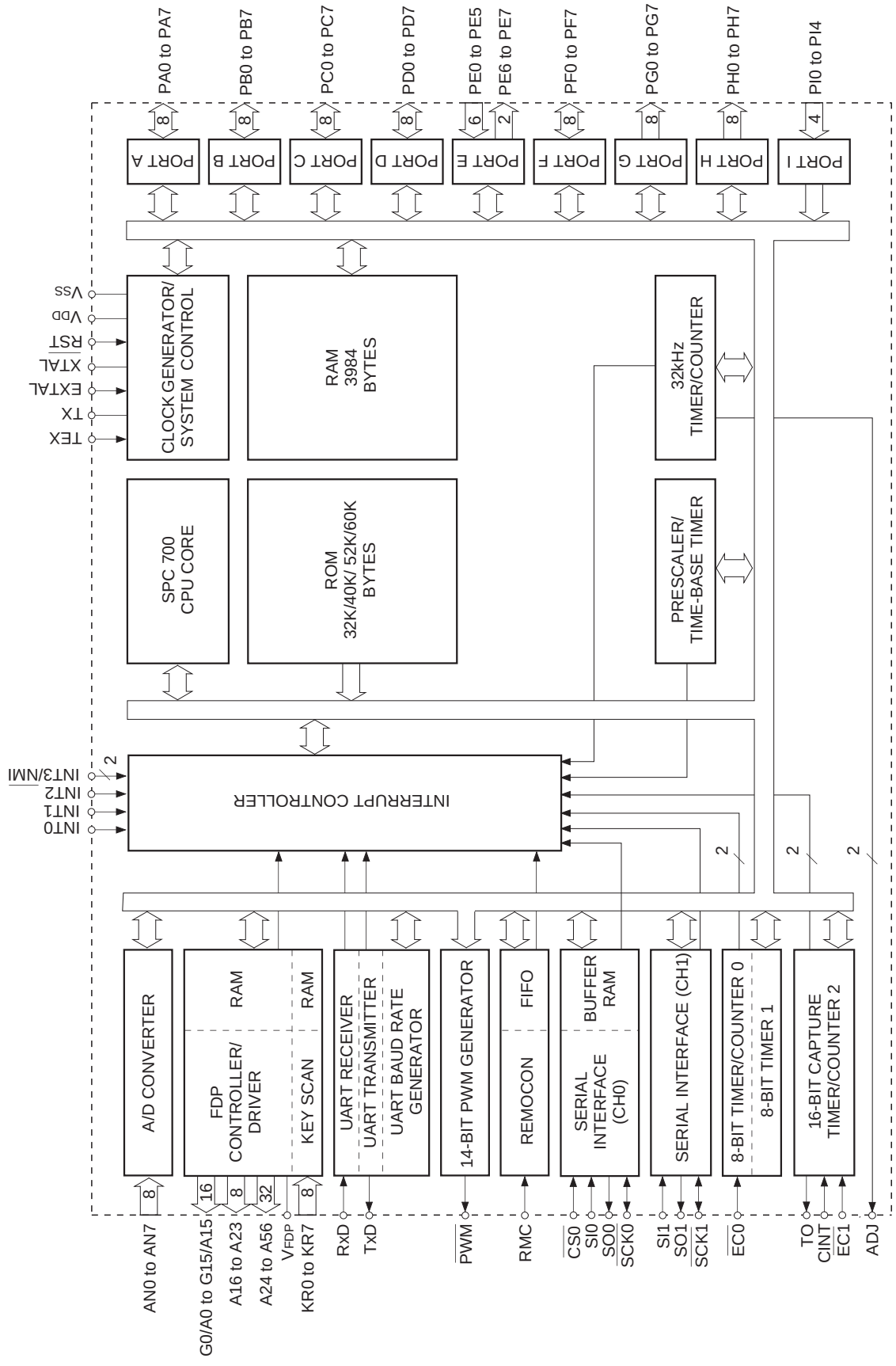
Silicon gate CMOS IC

Features

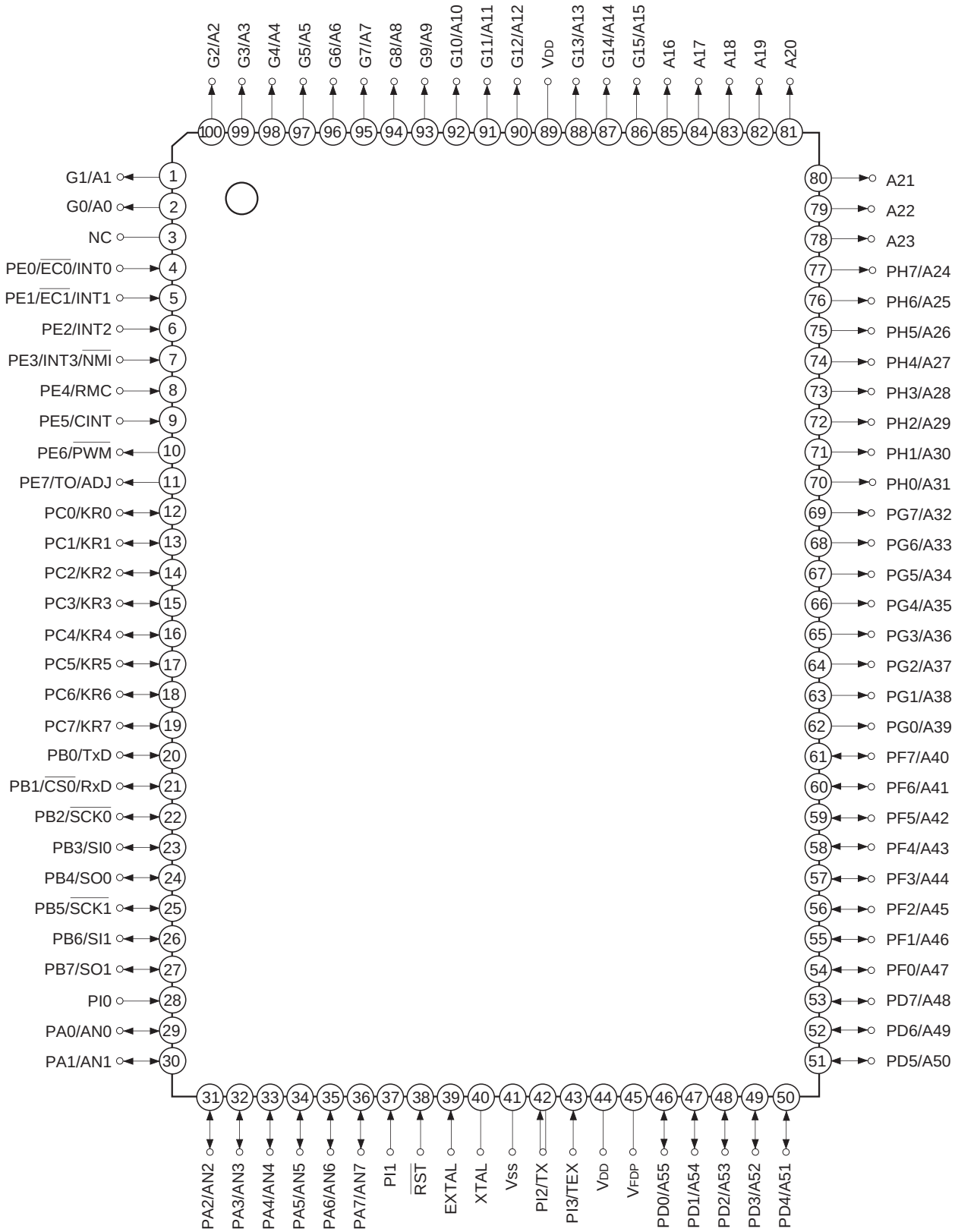
- Wide-range instruction system (213 instructions) to cover various types of data
  - — 16-bit arithmetic/multiplication and division/boolean bit operation instructions
- Minimum instruction cycle — 250ns at 16MHz operation; 122µs at 32kHz operation
- Incorporated ROM capacity — 32k bytes (CXP82032); 40k bytes (CXP82040); 52K bytes (CXP82052); 60K bytes (CXP82060)
- Incorporated RAM capacity — 3984 bytes (including fluorescent display area)
- Peripheral functions
  - — A/D converter — 8 bits, 8 channels, successive approximation method (Conversion time of 3.25µs/16MHz)
  - — Serial interface — Buffer RAM incorporated (Auto transfer for 1 to 32 bytes), 1 channel; 8-bit clock synchronized type (MSB/LSB first selectable), 1 channel; Start-stop synchronized type (UART), 1 channel
  - — Timers — 8-bit timer, 8-bit timer/counter, 19-bit time-base timer; 16-bit capture timer/counter, 32kHz timer/counter
  - — Fluorescent display panel controller/driver — Supports the universal grid fluorescent display panel.; High voltage drive output port of 56 pins (40V); Maximum of 640 segments display possible; Display timing number of 1 to 20; Dimmer function; Incorporated pull-down resistor (Mask option); Hardware key scan function (Maximum of 16 × 8 key matrix supportable)
  - — Remote control reception circuit — 8-bit pulse measurement counter, 6-stage FIFO
  - — PWM output — 14 bits, 1 channel
- Interruption — 17 factors, 15 vectors, multi-interruption possible
- Standby mode — Sleep/stop
- Package — 100-pin plastic QFP
- Piggy/evaluation chip — CXP82000 100-pin ceramic QFP

E97413A95-PS

Block Diagram



Pin Assignment (Top View)



Note) 1. NC (Pin 3) is left open.

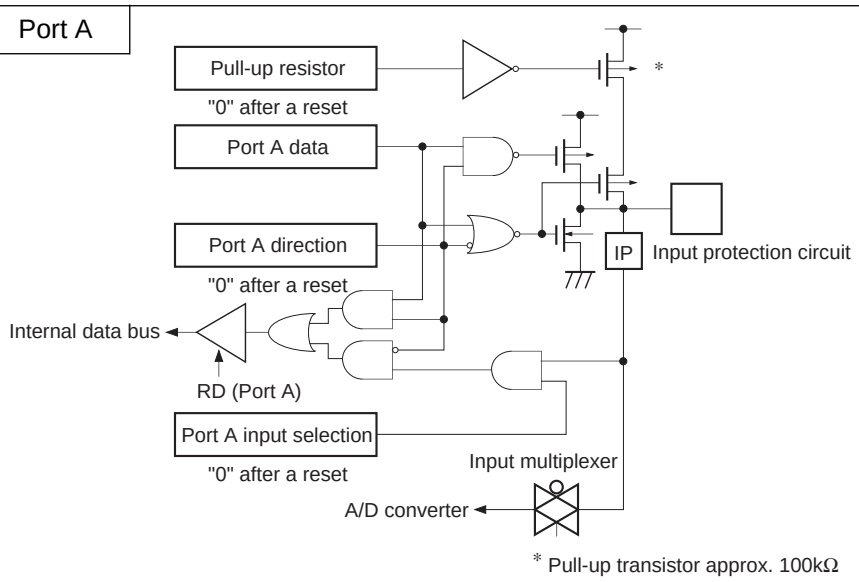
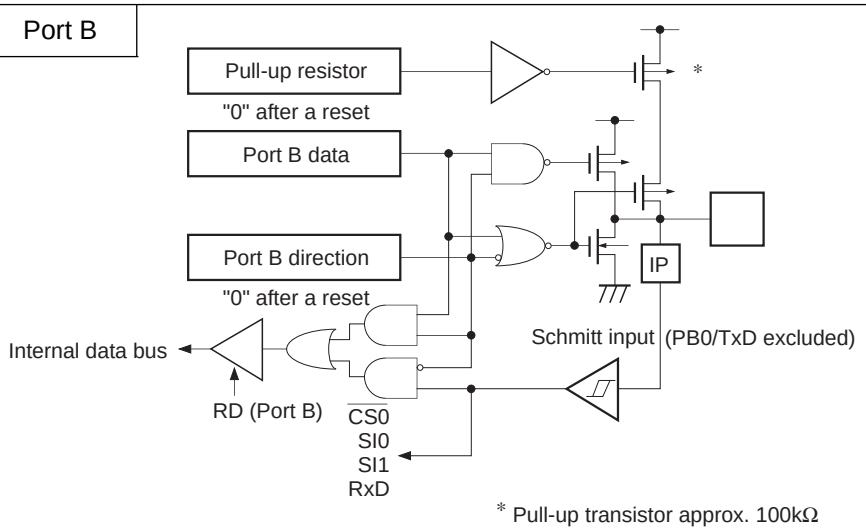
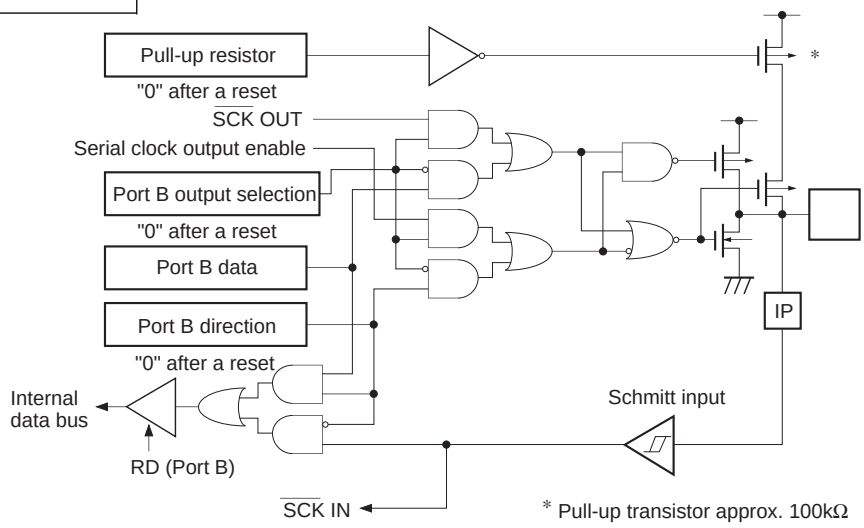
2. V_{DD} (Pins 44 and 89) must be connected to V_{DD}.

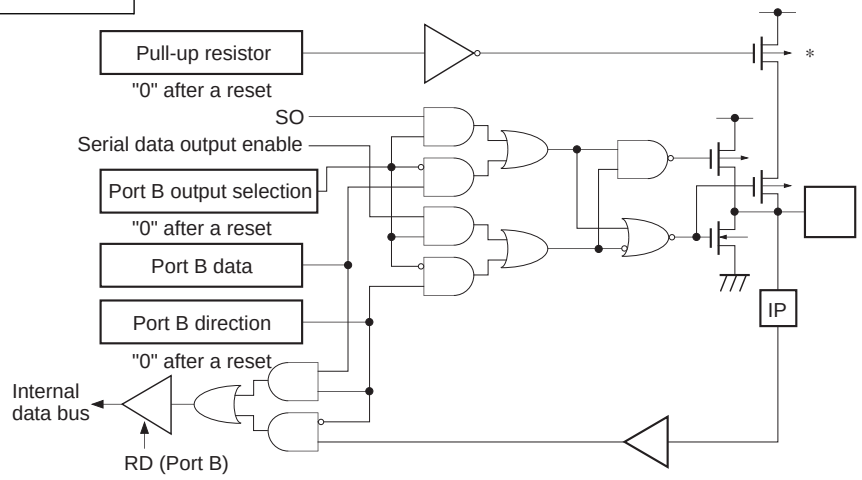
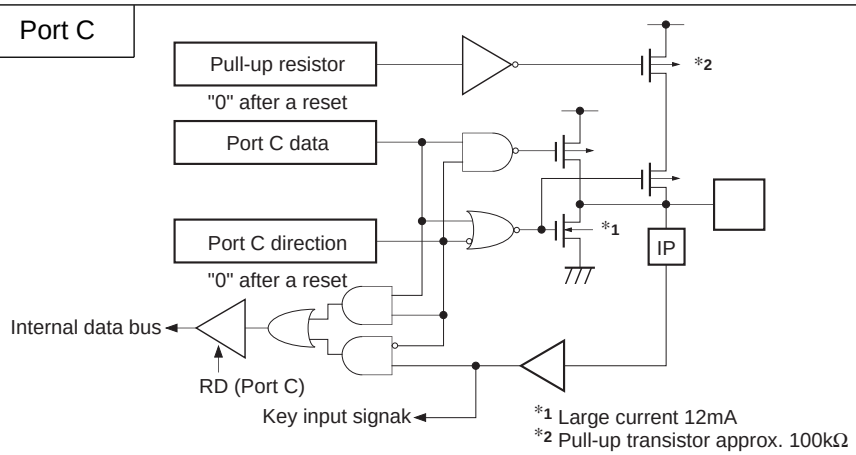
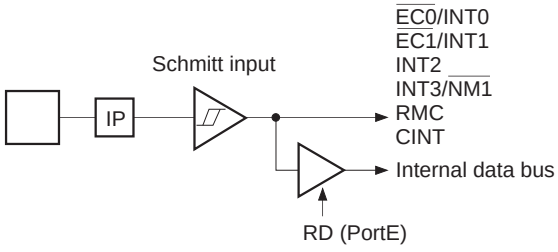
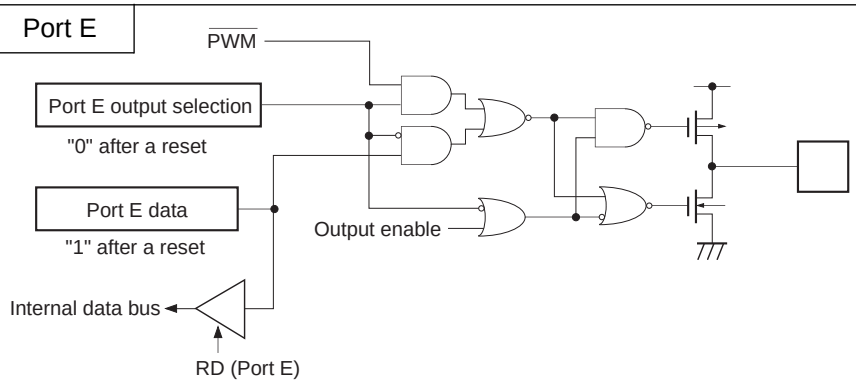
Pin Description

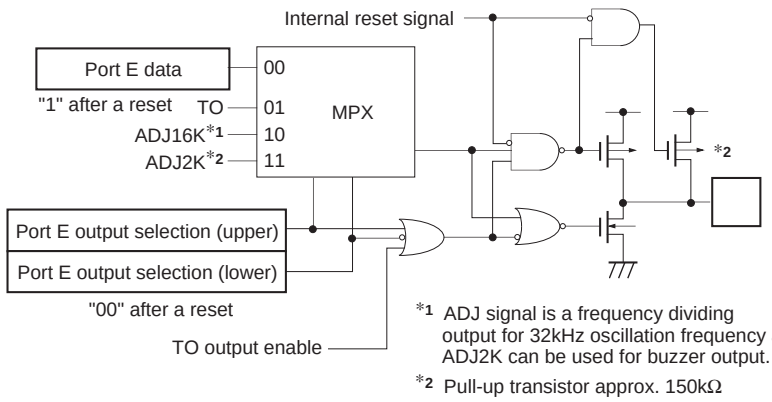
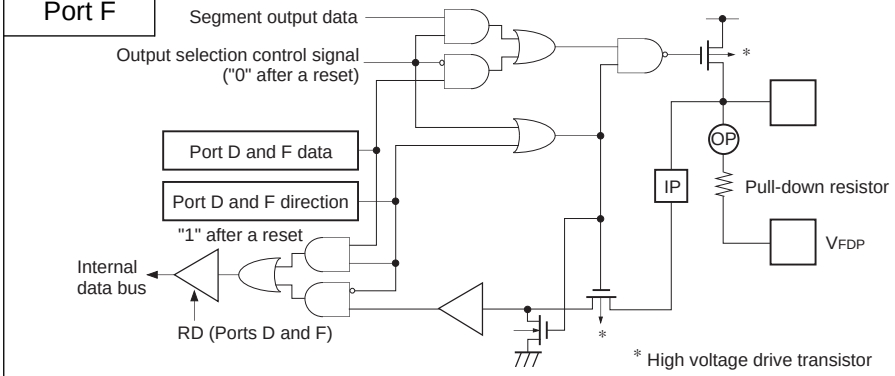
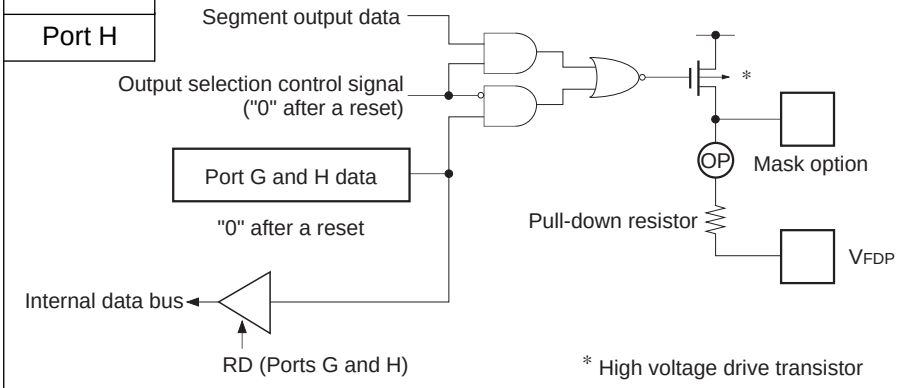
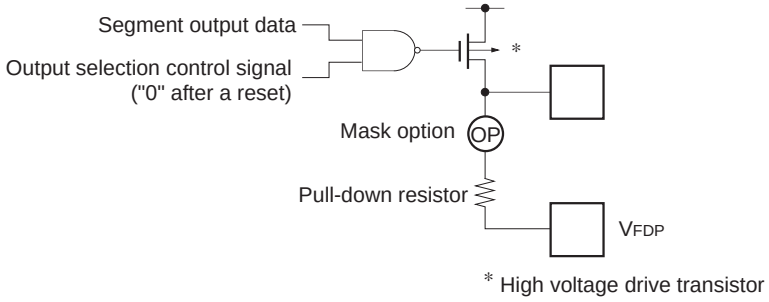
Symbol	I/O	Functions	
PA0/AN0 to PA7/AN7	I/O/ Analog input	(Port A) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of the pull-up resistor can be set through the program in a unit of 4 bits. (8 pins)	Analog inputs to A/D converter. (8 pins)
PB0/TxD	I/O/Output	(Port B) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of the pull-up resistor can be set through the program in a unit of 4 bits. (8 pins)	UART transmission data output.
PB1/$\overline{CS0}$/ RxD	I/O/Input/ Input		Chip select input for serial interface (CH0). / UART reception data input pin.
PB2/$\overline{SCK0}$	I/O/I/O		Serial clock I/O (CH0).
PB3/SI0	I/O/Input		Serial data input (CH0).
PB4/SO0	I/O/Output		Serial data output (CH0).
PB5/$\overline{SCK1}$	I/O/I/O		Serial clock I/O (CH1).
PB6/SI1	I/O/Input		Serial data input (CH1).
PB7/SO1	I/O/Output		Serial data output (CH1).
PC0/KR0 to PC7/KR7	I/O/Input	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Can drive 12mA sink current. Incorporation of the pull-up resistor can be set through the program in a unit of 4 bits. (8 pins)	Serves as key return inputs when operating key scan with fluorescent display panel (FDP) segment signal. (8 pins)
PD0/A55 to PD7/A48	I/O/Output	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)	FDP segment signal (anode connection) outputs.
$\overline{PE0}$/INT0/ $\overline{EC0}$	Input/Input/ Input	(Port E) 8-bit port. Lower 6 bits are for inputs; upper 2 bits are for outputs. (8 pins)	Inputs for external interruption request. (4 pins) / External event inputs for timer/counter. (2 pins)
$\overline{PE1}$/INT1/ $\overline{EC1}$	Input/Input/ Input		
PE2/INT2	Input/Input		
$\overline{PE3}$/INT3/ $\overline{NMI}$	Input/Input/ Input		Non-maskable interruption request input.
PE4/RMC	Input/Input		Remote control reception circuit input.
PE5/CINT	Input/Input		External capture input to 16-bit timer/counter.
PE6/$\overline{PWM}$	Output/Output		14-bit PWM output.
PE7/TO/ ADJ	Output/Output/ Output		Output for the 16-bit timer/counter rectangular waves, and 32kHz oscillation frequency division.

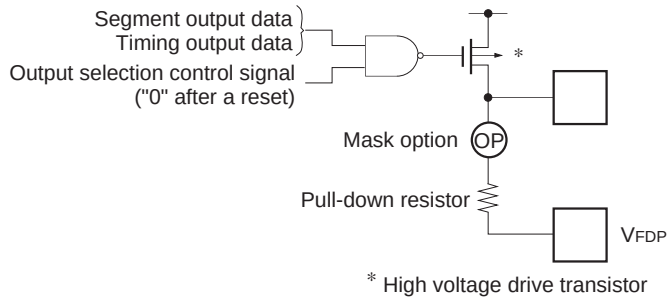
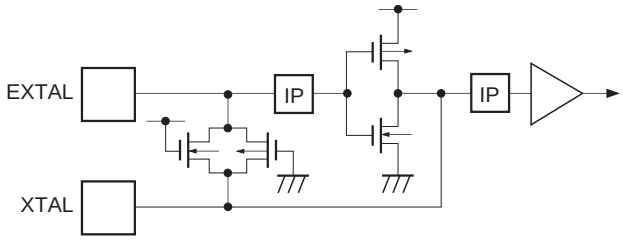
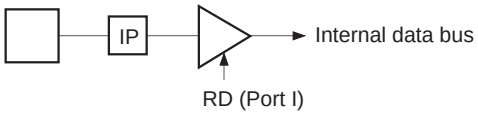
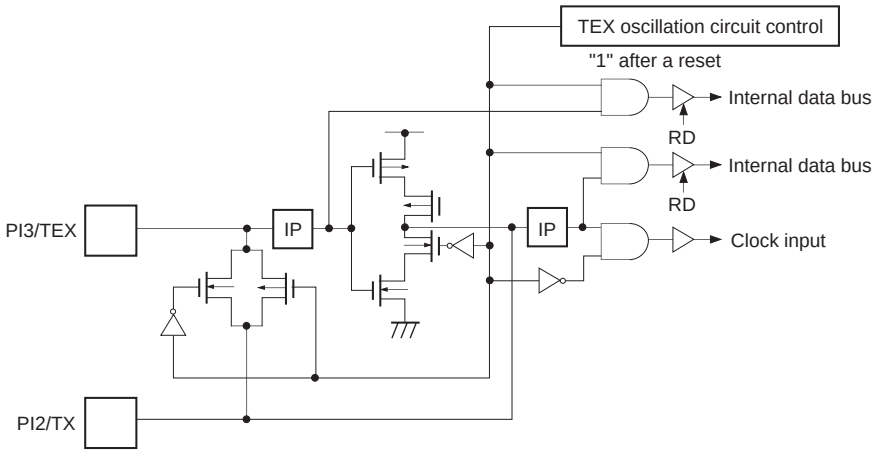
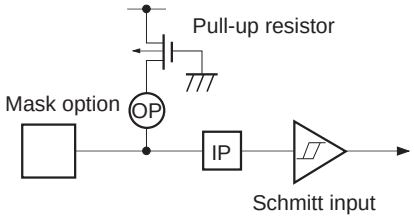
Symbol	I/O	Functions	
PF0/A47 to PF7/A40	I/O/Output	(Port F) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)	FDP segment signal (anode connection) outputs. (8 pins)
PG0/A39 to PG7/A32	Output/Output	(Port G) 8-bit output port. (8 pins)	FDP segment signal (anode connection) outputs. (8 pins)
PH0/A31 to PH7/A24	Output/Output	(Port H) 8-bit output port. (8 pins)	FDP segment signal (anode connection) outputs. (8 pins)
PI0	Input	(Port I) 4-bit input port. (4 pins)	
PI1	Input		
PI2/TX	Input		Crystal connectors for 32kHz timer/counter clock oscillation. For usage as event counter, input to TEX, and leave TX open.
PI3/TEX	Input/Input		
A16 to A23	Output	FDP segment signal (anode connection) outputs. (8 pins)	
G0/A0 to G15/A15	Output/Output	Outputs for FDP timing signals (grid connection)/segment signals (anode connection). (16 pins)	
V_{FDP}		FDP voltage supply when incorporated pull-down (PD) resistor is set by mask option.	
EXTAL	Input	Crystal connectors for system clock oscillation. When the clock is supplied externally, input to EXTAL; opposite phase clock should be input to XTAL.	
XTAL			
$\overline{RST}$	Input	Low-level active, system reset.	
NC		NC. Under normal operation, leave this pin open.	
V_{DD}		V_{CC} supply.	
V_{SS}		GND.	

I/O Circuit Format for Pins

Pin	Circuit format	After a reset
PA0/AN0 to PA7/AN7 8 pins	Port A 	Hi-Z
PB0/TxD PB1/$\overline{CS0}$/RxD PB3/SI0 PB6/SI1 4 pins	Port B 	Hi-Z
PB2/$\overline{SCK0}$ PB5/$\overline{SCK1}$ 2 pins	Port B 	Hi-Z

Pin	Circuit format	After a reset
PB4/SO0 PB7/SO1 2 pins	Port B  * Pull-up transistor approx. 100kΩ	Hi-Z
PC0/KR0 to PC7/KR7 8 pins	Port C  *1 Large current 12mA *2 Pull-up transistor approx. 100kΩ	Hi-Z
PE0/$\overline{EC0}$/INT0 PE1/$\overline{EC1}$/INT1 PE2/INT2 PE3/INT3/$\overline{NMI}$ PE4/RMC PE5/CINT 6 pins	Port E  	Hi-Z
PE6/$\overline{PWM}$ 1 pin	Port E  	High level

Pin	Circuit format	After a reset
PE7/TO/ADJ 1 pin	Port E  *1 ADJ signal is a frequency dividing output for 32kHz oscillation frequency adjustment. ADJ2K can be used for buzzer output. *2 Pull-up transistor approx. 150kΩ	High level (High level at ON resistance of pull-up transistor during a reset)
PD0/A55 to PD7/A48 PF0/A47 to PF7/A40 16 pins	Port D Port F  * High voltage drive transistor	Hi-Z or Low level (when PD resistor is connected)
PG0/A39 to PG7/A32 PH0/A31 to PH7/A24 16 pins	Port G Port H  * High voltage drive transistor	Hi-Z or Low level (when PD resistor is connected)
A16 to A23 8 pins	 * High voltage drive transistor	Hi-Z or Low level (when PD resistor is connected)

Pin	Circuit format	After a reset
G0/A0 to G15/A15 16 pins		Hi-Z or Low level (when PD resistor is connected)
EXTAL XTAL 2 pins	 • Diagram shows circuit composition during oscillation. • Feedback resistor is removed and XTAL becomes High level during stop.	Oscillation
PI0 PI1 2 pins		Hi-Z
PI2/TX PI3/TEX 2 pins		Oscillation stop Port input
$\overline{\text{RST}}$ 1 pin		Low level

Absolute Maximum Ratings (Vss = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V_{DD}	–0.3 to +7.0	V	
FDP display supply voltage	V_{FDP}	–40*2 to +7.0*1	V	
Input voltage	V_{IN}	–0.3 to +7.0*1	V	
Output voltage	V_{OUT}	–0.3 to +7.0*1	V	
Display output voltage	V_{OD}	–40*2 to +7.0*1	V	
High level output current	I_{OH}	–5	mA	All pins excluding display outputs*3 (value per pin)
	I_{ODH1}	–15	mA	Display outputs A20 to A55 (value per pin)
	I_{ODH2}	–50	mA	Display outputs G0/A0 to G15/A15, and A16 to A19 (value per pin)
High level total output current	$\sum I_{OH}$	–30	mA	Total for all pins excluding display outputs
	$\sum I_{ODH}$	–120	mA	Total for all display outputs
Low level output current	I_{OL}	15	mA	Pins excluding large current output (value per pin)
	I_{OLC}	20	mA	Large current output pins*4 (value per pin)
Low level total output current	$\sum I_{OL}$	100	mA	Total for all output pins
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–55 to +150	°C	
Allowable power dissipation	P_D	600	mW	

*1 V_{IN}, V_{OUT} and V_{OD} must not exceed V_{DD} + 0.3V.

*2 V_{FDP} and V_{OD} must not exceed V_{DD} – 40V.

*3 Specifies output current of general-purpose I/O ports.

*4 The large current drive transistor is the N-CH transistor of Port C (PC).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (Vss = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V_{DD}	4.5	5.5	V	Guaranteed operation range during 1/2 and 1/4 frequency dividing operation mode
		3.5	5.5	V	During 1/16 frequency dividing operation mode or sleep mode
		2.7	5.5	V	Guaranteed operation range with TEX clock
		2.5	5.5	V	Guaranteed data hold range during stop
High level input voltage	V_{IH}	0.7V_{DD}	V_{DD}	V	*1
	V_{IHS}	0.8V_{DD}	V_{DD}	V	*2
	V_{IHH}	0.7V_{DD}	V_{DD}	V	*3
	V_{IHEX}	V_{DD} – 0.4	V_{DD} + 0.3	V	EXTAL*4
Low level input voltage	V_{IL}	0	0.3V_{DD}	V	*1
	V_{ILS}	0	0.2V_{DD}	V	*2
	V_{ILH}	0	0.7	V	*3
	V_{ILEX}	–0.3	0.4	V	EXTAL*4
Operating temperature	Topr	–20	+75	°C	

*1 Value for each pin of normal input port (PA,PB0, PB4, PB7, PC).

*2 Value of the following pins: $\overline{\text{RST}}$, CINT, $\overline{\text{CS0}}$/TxD, RxD, SI0, SI1, $\overline{\text{SCK0}}$, $\overline{\text{SCK1}}$, $\overline{\text{EC0}}$/INT0, $\overline{\text{EC1}}$/INT1, INT2, INT3/$\overline{\text{NMI}}$, RMC.

*3 Value of the following pins: PD, PF.

*4 Specifies only during external clock input.

Electrical Characteristics

DC Characteristics

(Ta = –20 to +75°C, V_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE6, PE7, PF to PH	V_{DD} = 4.5V, I_{OH} = –0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = –1.2mA	3.5			V
Low level output voltage	V_{OL}	PA to PC, PE6, PE7	V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PC	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	µA
	I_{ILE}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.5		–40	µA
	I_{IHT}	TEX	V_{DD} = 5.5V, V_{IL} = 5.5V	0.1		10	µA
	I_{ILT}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.1		–10	µA
	I_{ILR}	$\overline{RST}$*1	V_{DD} = 5.5V, V_{IL} = 0.4V	–1.5		–400	µA
	I_{IL}	PA to PC*2				–50	µA
			V_{DD} = 4.5V, V_{IL} = 4.0V	–3.3			µA
Display output current	I_{OH}	A20 to A55	V_{DD} = 4.5V V_{OH} = V_{DD} –2.5V	–8			mA
		G0/A0 to G15/A15 A16 to A19		–30			mA
Open drain output leakage current (P-CH Tr off state)	I_{LOL}	G0/A0 to G15/A15 A16 to A55	V_{DD} = 5.5V V_{OL} = V_{DD} – 35V V_{FDP} = V_{DD} – 35V			–20	µA
Pull-down resistor*3	R_L	G0/A0 to G15/A15 A16 to A55	V_{DD} = 5V V_{OD} – V_{FDP} = 30V	30	70	220	kΩ
I/O leakage current	I_{IZ}	PA to PC*2, PD*4,PE0 to PE5,PF*4,PI, $\overline{RST}$*1	V_{DD} = 5.5V V_I = 0, 5.5V			±10	µA

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Power supply current*5	I_{DD1}	V_{DD}	1/2 frequency dividing operation mode V_{DD} = 5.5V, 16MHz crystal oscillation (C_1 = C_2 = 15pF)		23	50	mA
	I_{DD2}		V_{DD} = 3V, 32kHz crystal oscillation (C_1 = C_2 = 47pF)		30	100	µA
	I_{DDS1}		Sleep mode V_{DD} = 5.5V, 16MHz crystal oscillation (C_1 = C_2 = 15pF)		1.2	8	mA
	I_{DDS2}		V_{DD} = 3V, 32kHz crystal oscillation (C_1 = C_2 = 47pF)		12	30	µA
	I_{DDS3}		Stop mode V_{DD} = 5.5V, termination of 16MHz and 32kHz crystal oscillation			10	µA
Input capacity	C_{IN}	PA to PC, PD*4, PE0 to PE5, PF*4, PI, EXTAL, TEX, $\overline{RST}$	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

*1 $\overline{RST}$ specifies the input current when pull-up resistor has been selected; leakage current when no resistor has been selected.

*2 PA to PC pins specify the input current when pull-up resistor has been selected; leakage current when no resistor has been selected.

*3 When incorporated pull-down resistor has been selected through mask option.

*4 PD and PF pins are used as inputs by program. They specify pull-down resistor when no resistor has been selected by mask option.

*5 When all pins are open.

AC Characteristics

(1) Clock timing

(Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, Fig. 2	1		16	MHz
System clock input pulse width	t_{XL} t_{XH}	EXTAL	Fig. 1, Fig. 2 External clock drive	28			ns
System clock input rise time, fall time	t_{CR} t_{CF}	EXTAL	Fig. 1, Fig. 2 External clock drive	$t_{sys}+50$*1		200	ns
Event count input clock pulse width	t_{EH} t_{EL}	$\overline{EC0}$, $\overline{EC1}$	Fig. 3				ns
Event count input clock rise time, fall time	t_{ER} t_{EF}	$\overline{EC0}$, $\overline{EC1}$	Fig. 3			20	ms
System clock frequency	f_C	TEX TX	V_{DD} = 2.7 to 5.5V Fig. 2 (32kHz clock applied condition)		32.768		kHz
Event count input pulse width	t_{TL} t_{TH}	TEX	Fig. 3	10			µs
Event count input rise time, fall time	t_{TR} t_{TF}	TEX	Fig. 3			20	ms

*1 t_{sys} indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (CLC: 00FEh).
t_{sys} [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

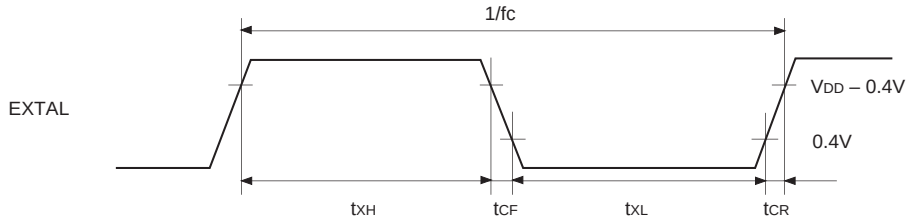


Fig. 1. Clock timing

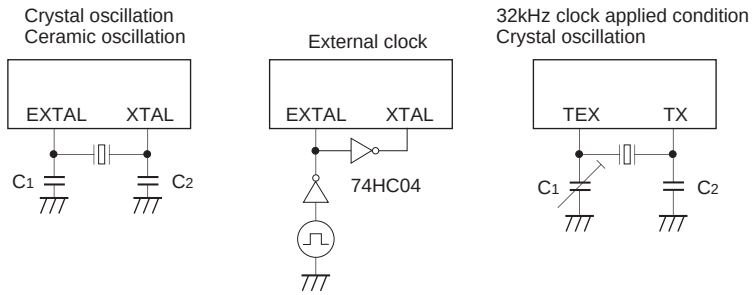


Fig. 2. Clock applied conditions

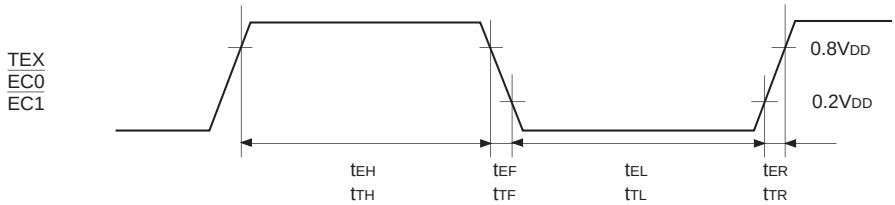


Fig. 3. Event count clock timing

(2) Serial transfer (CH0) (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Max.	Unit
$\overline{CS0} \downarrow \rightarrow \overline{SCK0}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		tsys + 200	ns
$\overline{CS0} \uparrow \rightarrow \overline{SCK0}$ float delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		tsys + 200	ns
$\overline{CS0} \downarrow \rightarrow$ SO0 delay time	t_{DCSO}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS0} \uparrow \rightarrow$ SO0 float delay time	t_{DCSOF}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS0}$ High level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	tsys + 200		ns
$\overline{SCK0}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	2tsys + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK0}$ High, Low level width	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	tsys + 100		ns
			Output mode	8000/fc – 50		ns
SI0 input set-up time (for $\overline{SCK0} \uparrow$)	t_{SIK}	SI0	$\overline{SCK0}$ input mode	100		ns
			$\overline{SCK0}$ output mode	200		ns
SI0 input hold time (for $\overline{SCK0} \uparrow$)	t_{KSI}	SI0	$\overline{SCK0}$ input mode	tsys + 200		ns
			$\overline{SCK0}$ output mode	100		ns
$\overline{SCK0} \downarrow \rightarrow$ SO0 delay time	t_{KSO}	SO0	$\overline{SCK0}$ input mode		tsys + 200	ns
			$\overline{SCK0}$ output mode		100	ns

Note 1) tsys indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (CLC: 00FEh).

tsys [ns] = 2000/fc (upper two bits = "00"), 4000/fc (upper two bits = "01"), 16000/fc (upper two bits = "11")

Note 2) The load condition for the $\overline{SCK0}$ output mode, SO0 output delay time is 50pF + 1TTL.

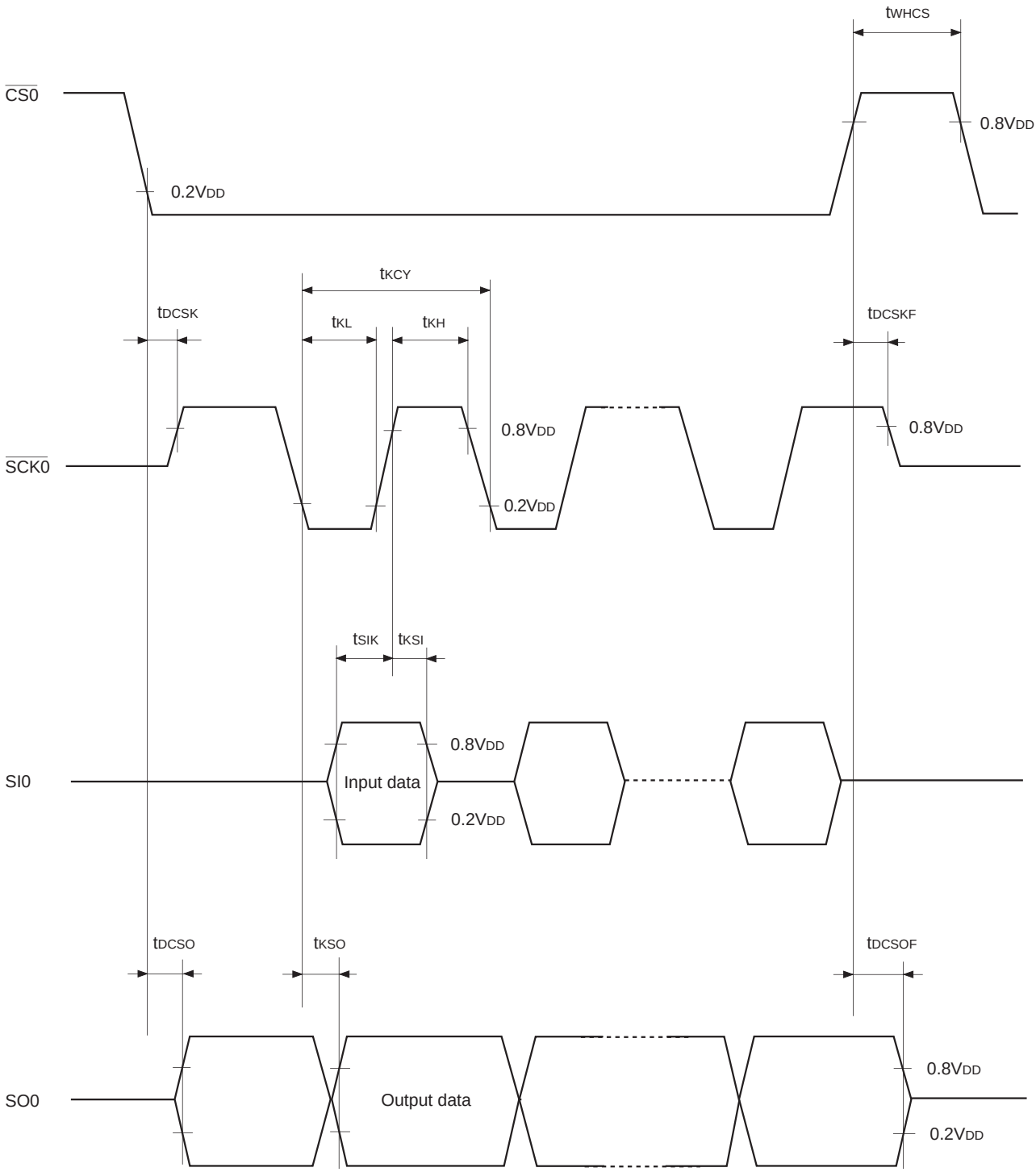


Fig. 4. Serial transfer CH0 timing

Serial transfer (CH1) (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
SCK1 cycle time	t_{KCY}	SCK1	Input mode	1000		ns
			Ouput mode	16000/fc		ns
SCK1 High, Low level width	t_{KH} t_{KL}	SCK1	Input mode	400		ns
			Ouput mode	8000/fc – 50		ns
SI1 input set-up time (for SCK1 ↑)	t_{SIK}	SI1	SCK1 input mode	100		ns
			SCK1 ouput mode	200		ns
SI1 input hold time (for SCK1 ↑)	t_{KSI}	SI1	SCK1 input mode	200		ns
			SCK1 ouput mode	100		ns
SCK1 ↓ → SO1 delay time	t_{KSO}	SO1	SCK1 input mode		200	ns
			SCK1 ouput mode		100	ns

Note) The load condition for the $\overline{SCK1}$ output mode, SO1 output delay time is 50pF + 1TTL.

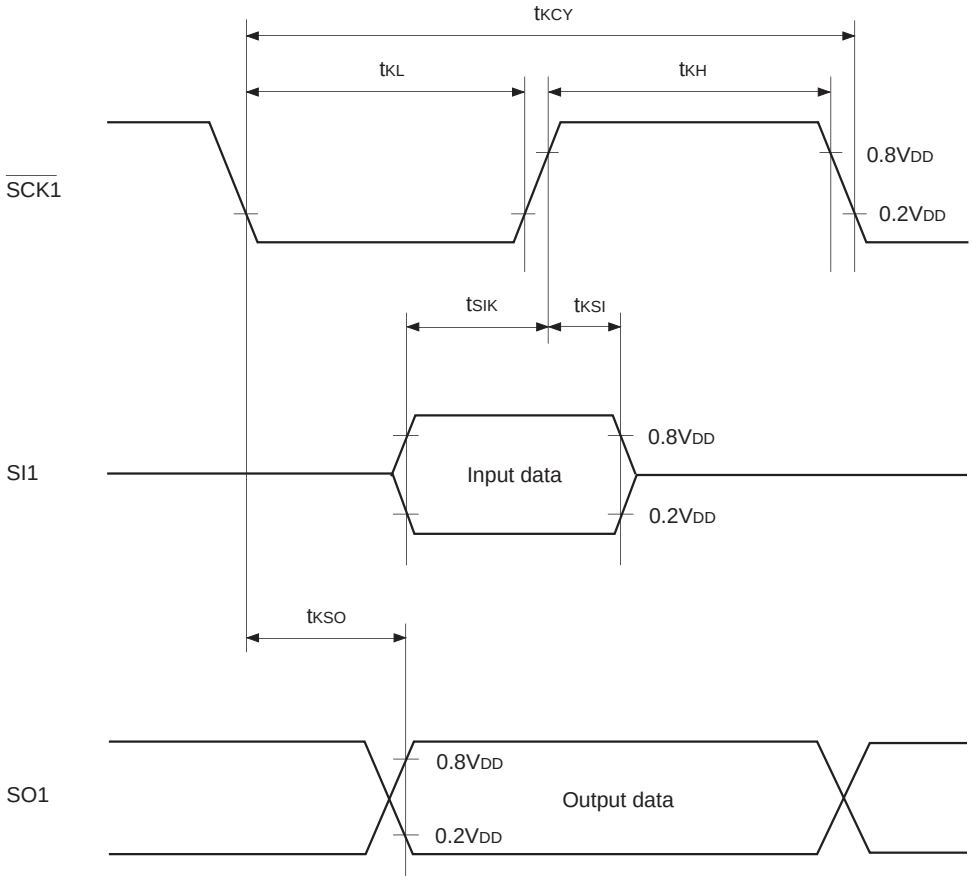
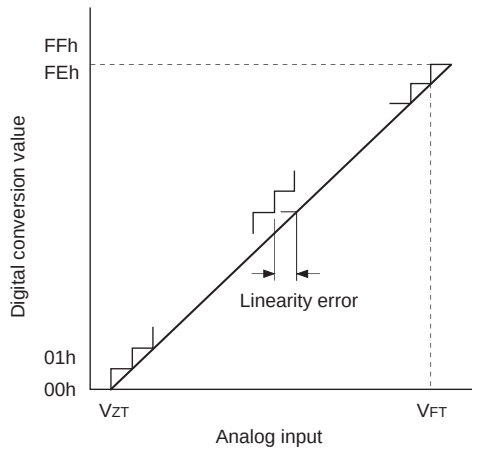


Fig. 5. Serial transfer CH1 timing

(3) A/D converter characteristics

(Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C V_{DD} = 5.0V V_{SS} = 0V			±3	LSB
Zero transition voltage	V_{ZT}*1			–10	10	70	mV
Full-scale transition voltage	V_{FT}*2			4910	4970	5030	mV
Conversion time	t_{CONV}			26/f_{ADC}*3			µs
Sampling time	t_{SAMP}			6/f_{ADC}*3			µs
Analog input voltage	V_{IAN}	AN0 to AN7		0		V_{DD}	V



*1 V_{ZT}: Value at which the digital conversion value changes from 00h to 01h and vice versa.

*2 V_{FT}: Value at which the digital conversion value changes from FEh to FFh and vice versa.

*3 f_{ADC} indicates the below values due to the contents of bit 6 (CKS) of the A/D control register (ADC: 00F9h) and bits 7 (PCK1) and 6 (PCK0) of the clock control register (CLC: 00FEh).

f_{ADC} = fc (CKS = "0"), fc/2 (CKS = "1")

However, the selection for f_{ADC} = fc (CKS = "0") is limited in the clock range of fc = 1 to 14MHz (V_{DD} = 4.5 to 5.5V).

Fig. 6. Definition of A/D converter terms

(4) Interruption, reset input (Ta = –20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption High, Low level width	t_{IH} t_{IL}	INT0 INT1 INT2 $\overline{NMI}$/INT3		1		µs
Reset input Low level width	t_{RSL}	$\overline{RST}$		32/fc		µs

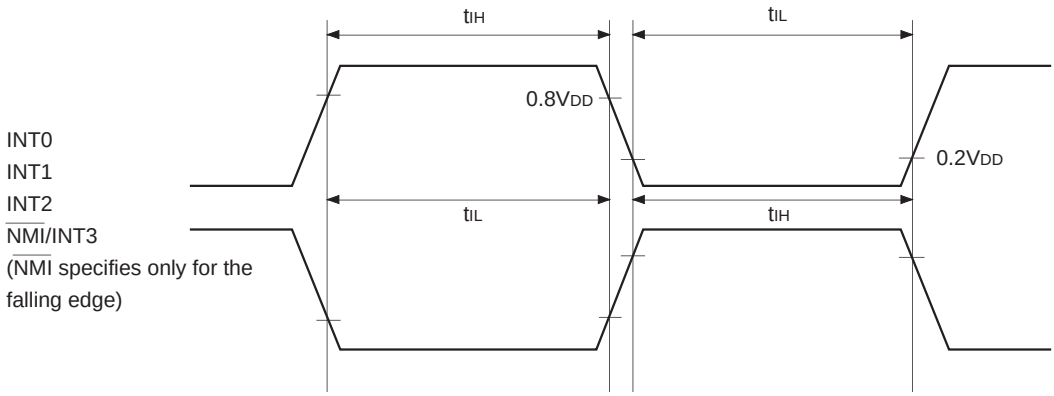


Fig. 7. Interruption input timing

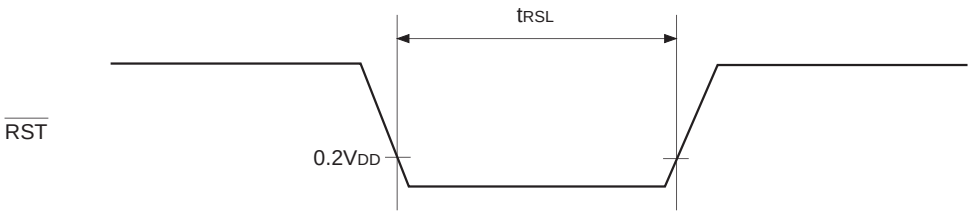


Fig. 8. $\overline{RST}$ input timing

Appendix

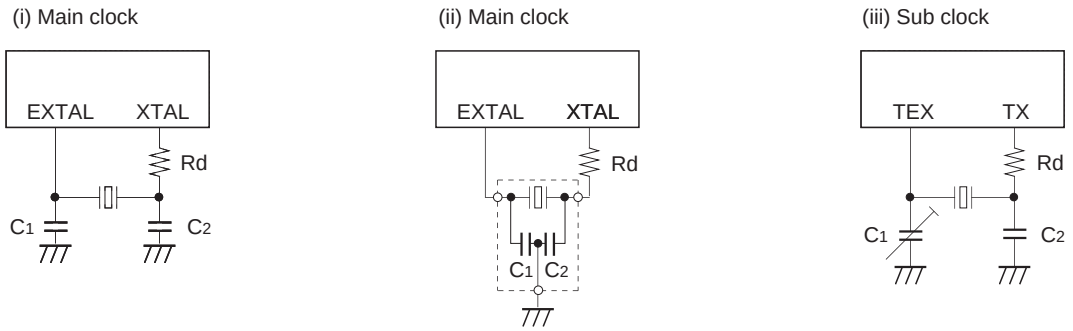


Fig. 9. Recommended oscillation circuit

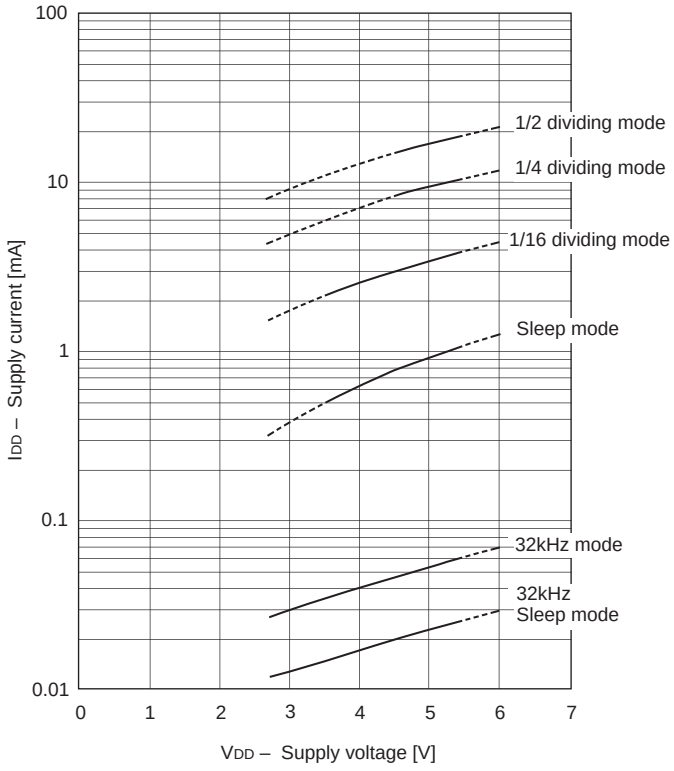
Manufacturer	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example	Remarks
MURATA MFG CO., LTD.	CSA10.0MTZ	10.0	30	30	0	(i)	
	CSA12.0MTZ	12.0					
	CSA16.00MXZ040	16.0	5	5			
	CST10.0MTW*	10.0	30	30		(ii)	
	CST12.0MTW*	12.0					
	CST16.00MXW0C1*	16.0	5	5			
RIVER ELETEC CO., LTD	HC-49/U03	8.0	18	18	330	(i)	
		12.0	12	12			
		16.0	10	10			
KINSEKI LTD.	HC-49/U (-S)	8.0	10	10	0		
		12.0	5	5			
		16.0	Open	Open			
Seiko Instruments Inc.	VTC-200 SP-T	32.768kHz	18	18	330k	(iii)	C_L = 12.5pF

Models marked with an asterisk (*) have the built-in ground capacitance (C_1, C_2).

Characteristics Curve

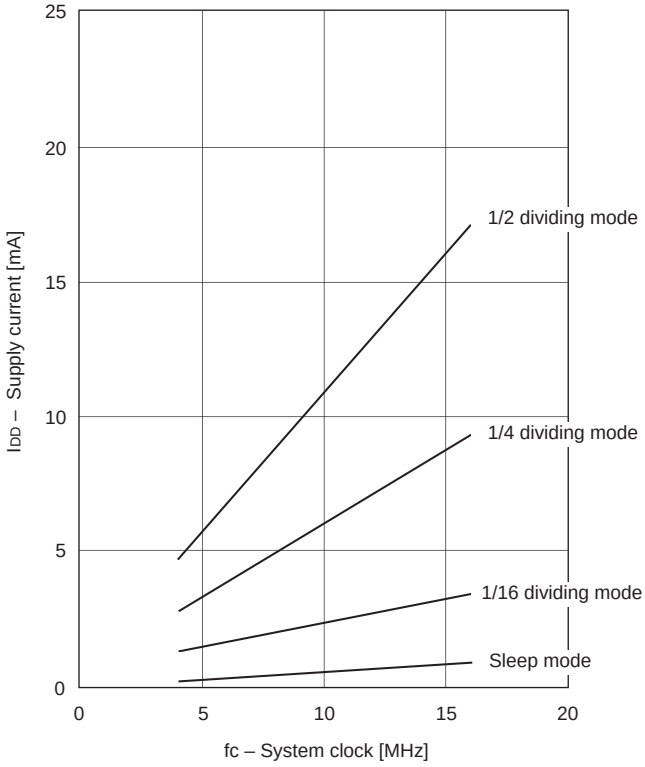
IDD vs. VDD

(Ta = 25°C, Typical)



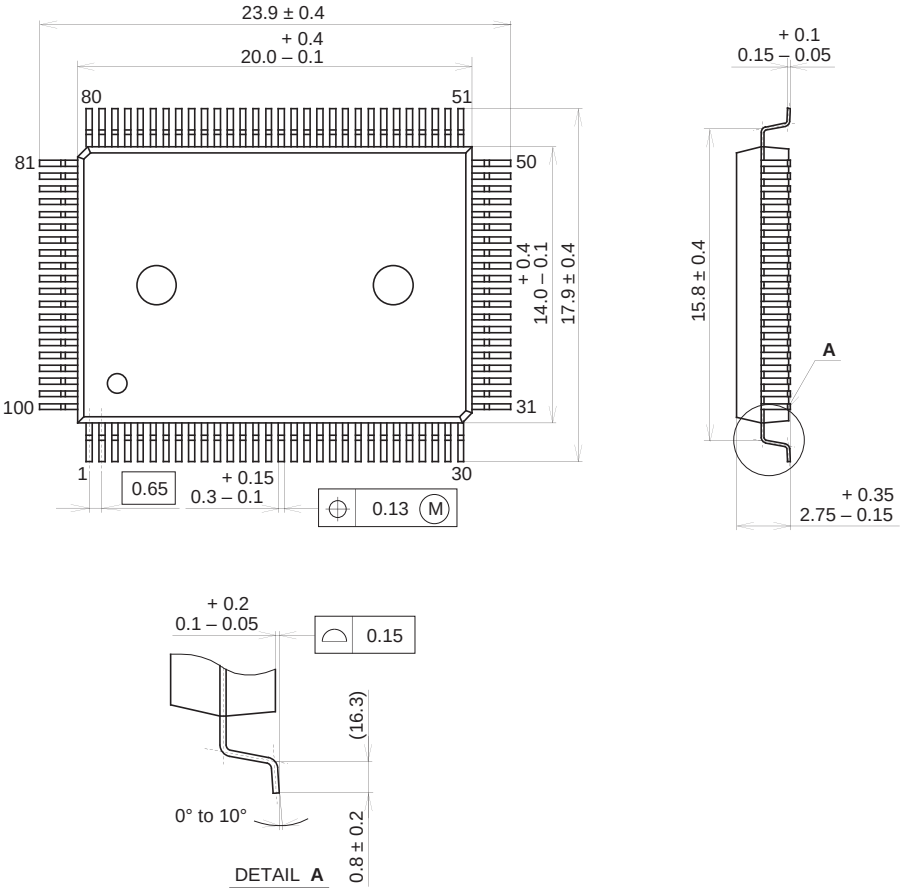
IDD vs. fc

(VDD = 5V, Ta = 25°C, Typical)



Package Outline Unit: mm

100PIN QFP (PLASTIC)



SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g